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BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER	
LEE, CHRISTOPHER E	
ART UNIT	PAPER NUMBER
2111	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/29/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/681,446	KOBAYASHI ET AL.	
	Examiner	Art Unit	
	Christopher E. Lee	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 February 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-61* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-30 and 32-39* is/are allowed.

6)☒ Claim(s) *40-42,45-51 and 54-61* is/are rejected.

7)☒ Claim(s) *31,43,44,52 and 53* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114 based on the Application No. 10/681,446, including the fee set forth in 37 CFR 1.17(e), was filed in this Application after final rejection, which the request is acceptable and an RCE has been established. Since this Application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office Action has been withdrawn pursuant to 37 CFR 1.114. Applicants' submission filed on 1st of February 2007 has been entered. Claims 1, 2, 5, 8, 26, 30, and 31 have been amended; no claim has been canceled; and no claim has been newly added since the Final Office Action was mailed on 11th of September 2006. Currently, claims 1-61 are pending in this Application.

Claim Objections

2. Claim 31 is objected to because of the following informalities:

It recites the subject matter "the second SMBase" in line 5. However, it has not been specifically clarified in the claim 31 and its intervening claims. Therefore, the Examiner presumes that the term "the second SMBase" could be considered as --the second SMBase address-- in light of the specification since it is not defined in the claims.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

4. Claims 54-59, and 61 are rejected under 35 U.S.C. 102(b) as being anticipated by Nguyen et al. [US 2002/0099893 A1; hereinafter Nguyen].

Referring to claim 54, Nguyen discloses an system (i.e., system for handling of system management interrupts in a multiprocessor computer system; See Abstract) comprising:

- a memory (i.e., SMRAM memory space 78 in Fig. 3) with a first memory address (i.e., memory location for Operating code for SMI handler of Processor 12c in Fig. 1) having system management interrupt (SMI) code (i.e., said Operating code; See paragraphs [0005] and [0019]);
- a first processor (i.e., said Processor 12c of Fig. 1) to execute the SMI code when a SMI (i.e., SMI issued by chipset initiated by peripheral devices, e.g., keyboard, etc.) is received (in fact, said Operating code for SMI handler of Processor being executed for said initiating peripheral device; See paragraphs [0005] and [0006]); and
- a second processor (i.e., Processor 12b of Fig. 1) to execute the SMI code (See paragraph [0018], lines 13-28), if the SMI is software generated (i.e., if the SMI issued by chipset initiated by a Processor; See step 46 in Fig. 2, in fact, software SMI; See paragraph [0017], lines 21 through 27; actually, checking SMI signature in SMRAM 78 of Fig. 3).

Referring to claim 55, Nguyen teaches

- the first processor (i.e., Processor 12c in Fig. 1) has a first system management base (SMBase) address (i.e., address of SMRAM space 84 in Fig. 3).

Referring to claim 56, Nguyen teaches

- the second processor (i.e., Processor 12b in Fig. 1) has a second SMBase address (i.e., address of SMRAM space 82 in Fig. 3).

Referring to claim 57, Nguyen teaches

- the first memory address (i.e., memory location for Operating code for SMI handler of Processor 12c in Fig. 1) has an offset (i.e., a predetermined address at said memory location of said Operating code) from the first SMBase (i.e., from a starting address of SMRAM space 84 in Fig. 3; in fact, said Processor 12c is designated as default SMI handling processor, wherein said Operating code is located at said predetermined address; See paragraphs [0005], [0008], and [0019]).

Referring to claim 58, Nguyen teaches

- a target SMBase (i.e., memory location for Operating code for SMI handler of Processor 12c in Fig. 1) referenced by the SMI code (i.e., accessed by said Operating code), by default, (i.e., a predetermined address at said memory location of said Operating code) is the first SMBase (i.e., address of SMRAM space 84 in Fig. 3 because said Processor 12c is designated as default SMI handling processor; See paragraph [0019]).

Referring to claim 59, Nguyen teaches

- the target SMBase is changed to the second SMBase (i.e., from SMRAM space 84 to SMRAM space 82 in Fig. 3 for Processor 12b of Fig. 1) before the second processor (i.e., said Processor 12b) executes the SMI code (See paragraphs [0018]-[0020]; in fact, a default SMI handling Processor 12c executes Operating code for SMI handler of Processor 12b in Fig. 1, which is actually the SMI code).

Referring to claim 61, Nguyen teaches

- the first and second processors (i.e., Processor 12c and Processor 12b in Fig. 1) are physical processors (See paragraph [0016], lines 1-5).

5. Claims 45, and 47-49 are rejected under 35 U.S.C. 102(a) as being anticipated by Dale [GB 2 382 180; cited by the Applicants].

Referring to claim 45, Dale discloses a system (i.e., cellular communication device in Fig.3) comprising:

- a controller hub (i.e., GSM ULPD 314 of Fig. 3) to generate a first system management interrupt (SMI; i.e., initiating signal for waking up process; See Steps 405-415 in Fig. 4, in fact, RF_Module 340 receiving RF_RADIO_ON signal 370 in Fig. 3; See page 18, lines 6-11);
- a memory (i.e., Memory 350 of Fig. 3) with a first memory address (i.e., memory element in said Memory) that contains code (i.e., waking up process; See page 20, lines 15-23);
- a first processor (i.e., GSM Processor 312 of Fig. 3) coupled to the controller hub (actually, said GSM Processor being coupled to said GSM ULPD in Fig. 3) to handle the first SMI (i.e., said waking up process), wherein
    - the first processor executes the code at the first memory address and generates a wake-up signal (in fact, said interrupt signal was caused by said RF_RADIO_ON signal from GSM Sub-system 310 in Fig. 3; See page 18, lines 27-30); and
- a second processor (i.e., MMI Processor 322 of Fig. 3) coupled to the controller hub (actually, said MMI Processor being coupled to said GSM ULPD via GPIO 321 in Fig. 3)

to handle the first SMI (i.e., said waking up process) after receiving the wake-up signal (See page 16, line 28 through page 17, line 2), wherein

- the second processor (i.e., said MMI Processor) executes the code at the first memory address (See page 18, lines 30-31 and page 19, lines 1-4).

Referring to claim 47, Dale teaches

- the first and second processors (i.e., GSM 312 and MMI 322 Processors in Fig. 3) are physical processors (See page 12, lines 5-6, and 15) located on separate packages (i.e., said GSM Processor 312 is packaged within GSM Sub-system 310, and said MMI Processor is packaged within MMI Sub-system 320 in Fig. 3; See page 12, lines 5-6, and 15).

Referring to claim 48, Dale teaches

- a pin (i.e., output pin from GSM ULPD 314 in Fig. 3) is toggled (i.e., RF_RADIO_ON signal 370 being set/reset in Fig. 3) on the controller hub (i.e., said GSM ULPD) to generated the first SMI (i.e., GSM ULPD 314 of Fig. 3 generates the SMI, which is an initiating signal for waking up process; See Steps 405-415 in Fig. 4).

Referring to claim 49, Dale teaches

code (i.e., Steps 405-415 in Fig. 4) is executed by the controller hub (i.e., GSM ULPD 314 of Fig. 3) to generate the first SMI (i.e., said GSM ULPD generates the SMI, which is an initiating signal for waking up process; See page 18, lines 6-14).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 40 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dale [GB 2 382 180] in view of Nalawadi [US 2003/0009654 A1].

Referring to claim 40, Dale discloses an apparatus (i.e., cellular communication device in Fig.3) comprising:

- a controller (i.e., GSM ULPD 314 of Fig. 3) to generate a first system management interrupt (SMI; i.e., initiating signal for waking up process; See Steps 405-415 in Fig. 4, in fact, RF_Module 340 receiving RF_RADIO_ON signal 370 in Fig. 3; See page 18, lines 6-11);
- a first logical processor (i.e., GSM Processor 312 of Fig. 3), coupled to the controller (actually, said GSM Processor being coupled to said GSM ULPD in Fig. 3), to handle the first SMI (i.e., said waking up process) and generate a wake-up signal (in fact, said

interrupt signal was caused by said RF_RADIO_ON signal from GSM Sub-system 310 in Fig. 3; See page 18, lines 27-30), wherein

- the wake-up signal (i.e., said interrupt signal for waking up MMI Processor) references (i.e., fetches) a first memory address of a default SMI handler (i.e., memory element having instructions in Memory 350 in Fig. 3, which is executed by said GSM Processor at Step 490 in Fig. 4; See page 21, lines 9-14); and

- a second logical processor (i.e., MMI Processor 322 of Fig. 3), coupled to the controller (actually, said MMI Processor being coupled to said GSM ULPD via GPIO 321 in Fig. 3), to handle the first SMI (i.e., said waking up process) after the wake-up signal is received from the first logical processor (See page 16, line 28 through page 17, line 2).

Dale does not teach that the first and second processors are logical processors.

Nalawadi discloses a computer system having a single processor equipped to serve as multiple logical processors (See Abstract), wherein

- a physical processor (i.e., Intel® Pentium® Family Processor, e.g., Intel® Pentium® 4 Processor; See paragraph [0006], lines 1-7) serving as a first and second logical processors (i.e., multiple logical processors; See paragraph [0006], lines 7-9).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted said first and second logical processors, as disclosed by Nalawadi, for said first and second processors (i.e., GSM and MMI Processors), as disclosed by Dale, for the advantage of providing a dual-processor (i.e., multiprocessor) capability for executing multiple-tasks in parallel using a single physical processor (See Nalawadi, paragraphs [0006]-[0007]).

Referring to claim 41, Dale teaches that handling the first SMI (i.e., initiating signal for waking up process) with the first logical processor (i.e., GSM Processor 312 of Fig. 3; See page 20, lines 15-23) comprises

- executing the default SMI handler (i.e., instructions being executed by said GSM Processor at Step 490 in Fig. 4) with the first logical processor (i.e., said GSM Processor; See page 21, lines 9-14).

9. Claim 42 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dale [GB 2 382 180] in view of Nalawadi [US 2003/0009654 A1] as applied to claims 40 and 41 above, and further in view of Rankin [US 5,613,071 A].

Referring to claim 42, Dale, as modified by Nalawadi, discloses all the limitations of the claim 42, except that does not expressly teach that the first memory location is 1k aligned.

Rankin discloses a method for providing remote memory access in a massively parallel data processing system (See Abstract), wherein an atomic operation for said remote memory access comprising:

- a first memory address (i.e., said AOM Region) is 4k aligned (See col. 14, lines 14-27).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said atomic operation, as disclosed by Rankin, in said apparatus (i.e., cellular communication device), as disclosed by Dale, as modified by Nalawadi, for the advantage of providing support for said atomic operations on remote data through said first memory address being aligned (i.e., AOM memory; See Rankin, col. 14, lines 12-13).

Dale, as modified by Nalawadi and Rankin, does not expressly teach that said first memory location is aligned in 1k instead of 4k.

However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have set up said alignment in 1k, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art*. *In re Boesch,* 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

10. Claim 46 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dale [GB 2 382 180] as applied to claims 45, and 47-49 above, and further in view of Nalawadi [US 2003/0009654 A1].

Referring to claim 46, Dale discloses all the limitations of the claim 46, except that does not teach that both the first and second processors are logical processors located on the same die.

Nalawadi discloses a computer system having a single processor equipped to serve as multiple logical processors (See Abstract), wherein

- both first and second processors are logical processors located on the same die
- a physical processor (i.e., Intel® Pentium® Family Processor, e.g., Intel® Pentium® 4 Processor; See paragraph [0006], lines 1-7) serving as a first and second logical processors on the same die (i.e., multiple logical processors on said Intel® Pentium® 4 Processor; See paragraph [0006], lines 7-9).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted said first and second logical processors, as disclosed by Nalawadi, for said first and second processors (i.e., GSM and MMI Sub-systems), as disclosed by Dale, for the advantage of providing a dual-processor (i.e., multiprocessor) capability for

* Applicants' disclosure on page 13, paragraph [0038] states that the Applicants' invention is also picking up an optimum value from 1k, 4k, or other aligned memory address range without any particular purpose.

executing multiple-tasks in parallel using a single physical processor (See Nalawadi, paragraphs [0006]-[0007]).

11. Claims 50 and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dale [GB 2 382 180] as applied to claims 45, and 47-49 above, and further in view of Nguyen [US 2002/0099893 A1].

Referring to claim 50, Dale discloses all the limitations of the claim 50, except that does not teach the code at the first memory address is SMI handling code.

Nguyen discloses a system for handling of system management interrupts in a multiprocessor computer system (See Abstract), wherein

- code (i.e., Operating code for SMI handler of Processor 12c in Fig. 1) at a first memory address (i.e., memory location for said Operating code) is SMI handling code (i.e., software SMI handler; See paragraphs [0005] and [0019]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said handling of system management interrupts (i.e., software SMI handling), as disclosed by Nguyen, in said system, as disclosed by Dale, for the advantage of providing said handling of SMIs for said system (i.e., multiprocessor computer system) using only one or subset of processors (See Nguyen, paragraph [0010]).

Referring to claim 51, Dale teaches

- the wake-up signal (i.e., interrupt signal for waking up MMI Processor 322 of Fig. 3) is a vector (i.e., processor interrupt signal inherently anticipates the claimed subject matter "vector based") containing the first memory address (i.e., interruption signal generated for said MMI Processor; See page 18, line 27 through page 19, line 4).

12. Claim 60 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nguyen [US 2002/0099893 A1] as applied to claims 54-59, and 61 above, and further in view of Nalawadi [US 2003/0009654 A1].

Referring to claim 60, Nguyen discloses all the limitations of the claim 60, except that does not teach that the first and second processors are logical processors.

Nalawadi discloses a computer system having a single processor equipped to serve as multiple logical processors (See Abstract), wherein

- a physical processor (i.e., Intel® Pentium® Family Processor, e.g., Intel® Pentium® 4 Processor; See paragraph [0006], lines 1-7) serving as a first and second logical processors (i.e., multiple logical processors; See paragraph [0006], lines 7-9).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted said first and second logical processors, as disclosed by Nalawadi, for said first and second processors (i.e., Processors 12 in Fig. 1), as disclosed by Nguyen, for the advantage of providing a multiprocessor capability for executing multiple-tasks in parallel using a single physical processor (See Nalawadi, paragraphs [0006]-[0007]).

Allowable Subject Matter

13. Claims 1-30 and 32-39 are allowed.

14. Claim 31 would be allowable if rewritten or amended to overcome the claim 31 objection under minor informality, set forth in this Office action.

15. Claims 43, 44, 52, and 53 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

16. The following is a statement of reasons for the indication of allowable subject matter:

With respect to claim 1, the claim limitations are deemed allowable over the prior art of record as the prior art fails to teach or suggest that receiving a first system management interrupt (SMI) with a first and a second processor; handling the first SMI with the second processor; generating a wake-up signal with the first processor after receiving the first SMI; awakening the second processor, based on the wake-up signal from the first processor; and handling the first SMI with the second processor.

The claims 2-11 are dependent claims of the claim 1.

With respect to claim 12, the claim limitations are deemed allowable over the prior art of record as the prior art fails to teach or suggest that executing code at a first memory location with a first processor in response to the first SMI; and executing the code from the first memory location with the second processor, in response to the first SMI after awakening the second processor.

The claims 13-25 are dependent claims of the claim 12.

With respect to claim 26, the claim limitations are deemed allowable over the prior art of record as the prior art fails to teach or suggest that receiving a system management interrupt (SMI); executing a SMI handler on a first processor to handle the SMI for the first processor; and executing the SMI handler on a second processor to handle the SMI for the second processor.

The claims 27-31 are dependent claims of the claim 26.

With respect to claim 32, the Applicants' arguments (See the Response page 19, filed on 1st of February 2007) have been fully considered and are persuasive, and thus, the rejection of the claim 32 has been withdrawn. Furthermore, the claim limitations are deemed allowable over the prior art of record as the prior art fails to teach or suggest that checking if the SMI is a

software generated SMI; and executing the SMI code to handle the SMI for a second processor, if the SMI is software generated.

The claims 33-39 are dependent claims of the claim 32.

With respect to claim 43, the claim limitations are deemed allowable over the prior art of record as the prior art fails to teach or suggest that handling the first SMI with the second logical processor comprises executing the default SMI handler with the second logical processor.

The claim 44 is a dependent claim of the claim 43.

With respect to claim 52, the claim limitations are deemed allowable over the prior art of record as the prior art fails to teach or suggest that handling the first SMI with the second processor after receiving the wake-up signal comprising setting a pointer to a second memory address.

The claim 53 is a dependent claim of the claim 52.

Response to Arguments

17. Applicants' arguments filed 1st of February 2007 have been fully considered but they are not persuasive.

In response to the Applicants' argument with respect to the Claim 31 objection in the Response page 15, lines 4-10, the Examiner respectfully disagrees.

As the Applicants admitted, the claim 31 recites the subject matter "a second SMBase address" in lines 3-4. However, the claim 31 recites the language "the second SMBase" in line 5, which is clearly having a broader meaning than the language "the second SMBase address," and thus, the claiming language "the second SMBase" is in a lack of antecedent basis.

Thus, the Applicants' argument on this point is not persuasive.

In response to the Applicants' argument with respect to "Referring next to applicant's claim 45, ... However, Dale does not suggest the MMI processor and the GSM processor are to execute code at the same memory location, i.e. code at the first memory address. In contrast, the first processor and the second processor in applicant's claim 45 execute code from the first memory address. As Dale does not suggest or teach executing code at the same location with a first and a second processor, applicant respectfully submits that claim 45 and its dependent claims, 46-53 are now in condition for allowance." in the Response page 16, lines 13-23, the Examiner respectfully disagrees.

In fact, the claim 45 recites the limitations "a memory with a first memory address that contains code" in line 3, "the first processor executes the code at the first memory address" in lines 4-5, and "the second processor executes the code at the first memory address" in lines 8-9. In general, one of ordinary skill in the art of computer technologies understands that the claimed subject matter "code" being executed by a processor cannot be located at the specific memory address, i.e., at the first memory address, but should be located within a memory location starting with the specific memory address, in other words, the claimed subject matter "first memory address" should be interpreted as a memory location starting with the specific memory address to be executed by the first and second processors. Therefore, in contrary to the Applicants' assertion, i.e., the first processor and the second processor are to execute code at the same memory location, the Applicants claim that the first processor and the second processor execute code at the memory location starting with the specific memory address in the claim 45. In accordance with the above mentioned interpretation of the claim 45, Dale impliedly suggests the claimed limitations "a memory with a first memory address that contains code," "the first processor executes the code at the first memory address," and "the second processor executes the code at the first memory address," such that a Memory 350 with a range of

specific memory element that contains code of waking up process in Fig. 3 (See Dale, page 20, lines 15-23); the GSM Processor 312 executes the code of waking up process at the range of specific memory element for waking up process in Fig. 3 (See Dale, page 18, lines 27-30); and the MMI Processor 322 executes the code of waking up process at the range of specific memory element for waking up process in Fig. 3 (See Dale, page 18, lines 30-31 and page 19, lines 1-4).

Thus, the Applicants' argument on this point is not persuasive.

In response to the Applicants' argument with respect to "Examiner rejects claim 40 under U.S.C, 103 as being unpatentable over Dale in view of Nalawadi (US 2003.0009654 A1). However, claim 40 includes the limitation of 'a first logical processor ... to handle the first SMI and generate a wake-up signal after the first SMI. ... However, as stated above, Dale expressly teaches that the GPIO is in the MMI sub-system. ..." in the Response page 17, lines 1-16, the Examiner notices that that the features upon which applicants rely (i.e., a first logical processor ... to handle the first SMI and generate a wake-up signal after the first SMI) are not recited in the rejected claim 40. Although the claim is interpreted in light of the specification, limitations from the specification are not read into the claim 40. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Thus, the Applicants' argument on this point is not persuasive.

Conclusion

18. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Huang [US 6,711,642 B2] discloses method and chipset for system management mode interrupt of multi-processor supporting system.

Quimby et al. [US 5,978,903 A] disclose apparatus and method for automatically accessing a dynamic RAM for system management interrupt handling.

Tyner et al. [US 6,272,618 B1] disclose system and method for handling interrupts in a multi-processor computer.

Lewis [US 7,043,729 B2] discloses reducing interrupt latency while polling.

Bennett et al. [US 6,968,410 B2] disclose multi-threaded processing of system management interrupts.

Cooper et al. [US 7,152,169 B2] disclose method for providing power management on multi-threaded processor by using SMM mode to place a physical processor into lower power state.

Chang [US 6,775,734 B2] discloses memory access using system management interrupt and associated computer system.

Jain et al. [US 6,782,472 B2] method of initializing a memory controller by executing software in a second memory to wake up a system.

Chaiken et al. [US 6,792,480 B2] disclose status display being visible in a closed position and displaying a track number during play mode comprising a reduced power of a system.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 571-272-3637. The examiner can normally be reached on Monday through Friday, 9:30am - 6:00pm (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Christopher E. Lee
Primary Patent Examiner
Art Unit 2111

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